IDEC Chip Design Contest

An LDMOS-Based Temperature-Compensated Voltage Reference for EV BMS

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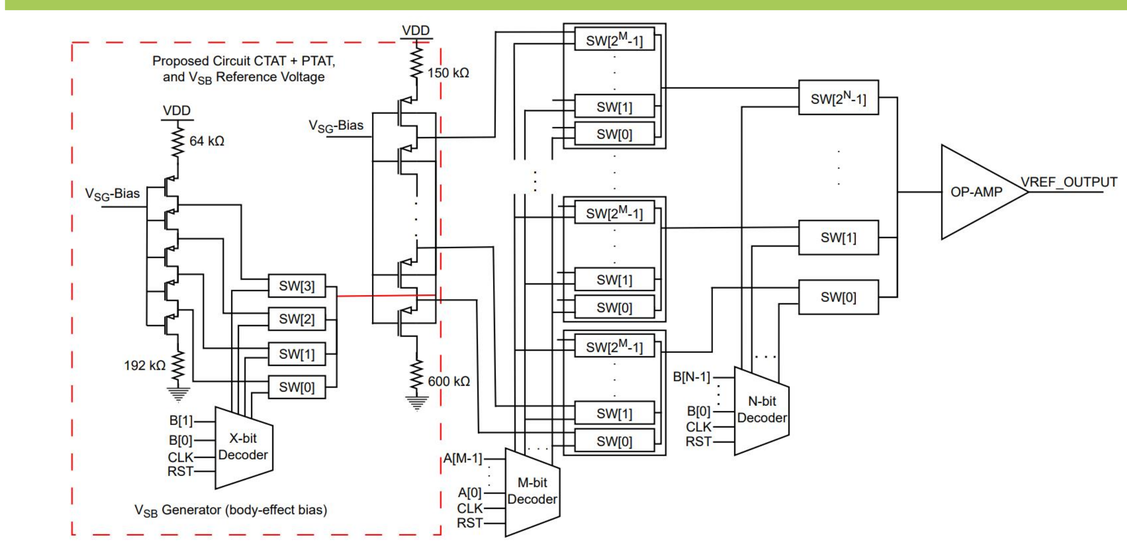
Abstract

This work presents a temperature-compensated voltage reference for EV BMS applications. LDMOS devices are attractive for such systems because they support high-voltage operation and robust performance. However, accurate cell-voltage monitoring still requires a highly stable reference, since reference drift directly translates into sensing error in ΔΣ ADC-based systems. To address this, the proposed stacked LDMOS triode-region voltage reference combines CTAT and PTAT current components, together with gate-width optimization and body-effect biasing, to suppress temperature drift. A two-stage coarse-fine decoder enables a programmable 3.2 – 4.2 V output with 1 mV resolution. Fabricated in a 180 nm high-voltage CMOS process, the circuit achieves a 0.3 mV variation from -20°C to 100°C, corresponding to 0.61 ppm/°C, within an active area of 0.0038 mm².

Motivation

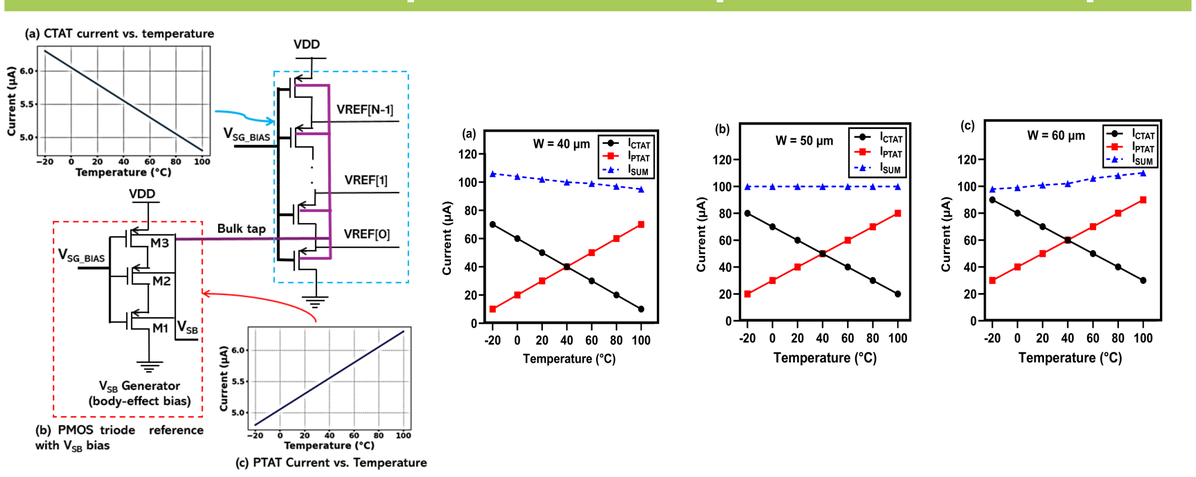
- LDMOS devices are attractive for EV BMS because they support high-voltage operation and robust performance.
- However, accurate cell-voltage monitoring still requires a highly stable reference voltage.
- In ΔΣ ADC-based systems, reference drift directly translates into cell-voltage error.
- This work therefore proposes a temperature-compensated programmable voltage reference with ultra-low drift for EV BMS applications.

Proposed Architecture



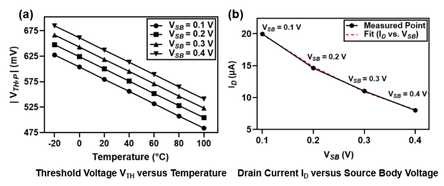
- Stacked LDMOS devices are placed near VDD so that each device operates in the triode region and produces a small, monotonic voltage drop.
- A V_{SB} generator provides body-bias tuning, while coarse and fine digital decoders trim the output to the desired reference voltage.

Gate-Width Temperature Compensation Principle

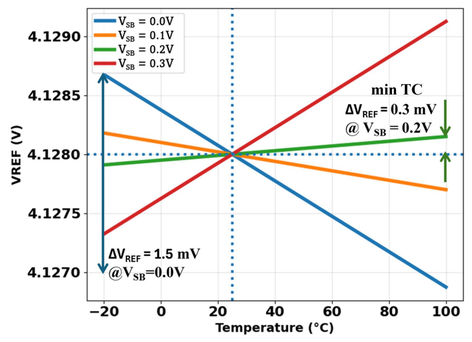


- In the weak-triode branch, the mobility term dominates, so the current decreases with temperature, CTAT behavior.
- In the deep-triode branch, the effective overdrive term dominates, so the current increases with temperature, resulting in PTAT behavior.
- *W* = 50 µm provides the flattest composite current, close to 100 µA over temperature.
- This width is selected before fine V_{SB}-based body-bias tuning.

Body-Bias Tuning for Temperature Compensation

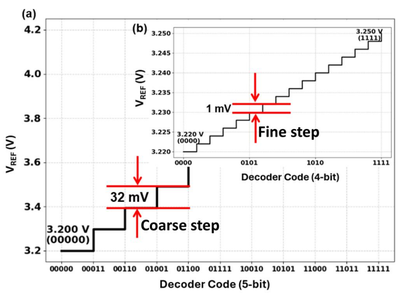


- V_{SB}-based body-bias tuning for temperature compensati on in the proposed reference ladder.

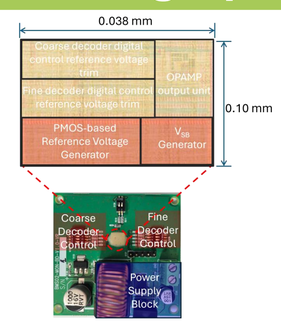


- Reference voltage vs temperature for different V_{SB} values.

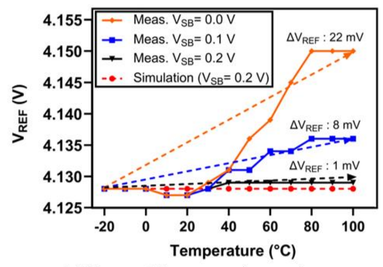
Measurement Result and Chip Micrograph



- Programmable reference voltage characteristic of the proposed reference ladder.



- Chip micrograph and evaluation board photograph.



(a) Measured V_{REF} versus temperature

(b) Temperature Chamber Measurement Setup

- Measured output versus temperature compensation under different body-bias voltage and temperature chamber measurement setup (photo)

Measured Performance and Comparison Table

Parameter	This Work	OJCAS [1]	ICCECE [2]	ACCESS [3]
Technology [nm]	180 high - Voltage CMOS	350	180	180
Power [µW]	27.2	NA	0.000176	0.0176
Temperature Range [°C]	-20 to 100	NA	0 to 100	-40 to 85
Fine Resolution[mV]	1	NA	NA	NA
Temperature coefficient [ppm/°C]	0.61	<15	13.06	35.7
Area, mm²	0.0038	NA	0.0048	0.0092

[1] Byambajav. Ragchaa, Liji. Wu, Xiangmin. Zhang, "A Design of Fault-Tolerant Battery Monitoring IC for Electric Vehicles Complying with ISO 26262," IEEE Open Journal of Circuits and Systems (OJCAS) (2024).
[2] K. Yu, Q. Hu, S. Li, " A 146pW, 0.4V, 0.015%/V Line Sensitivity, High PSRR Leakage-Biased CMOS Voltage Reference with the Optimization of Body Parasitic Effects," 4th In ternational Conference on Consumer Electronics and Computer Engineering (ICCECE), (2024).
[3] X. Tong, A. Yang and S. Dong, "A 17.6-nW 35.7-ppm/°C Temperature Coefficient All-SVTMOSFET Subthreshold Voltage Reference in Standard 0.18-µm N-Well CMOS," IEEE (Access), (2020).

Conclusion

- The proposed stacked LDMOS triode ladder realizes a directly programmable 3.2–4.2 V high-side reference with 1 mV trim resolution for BMS applications.
- Temperature drift is minimized by balancing CTAT weak-triode and PTAT deep-triode currents through width optimization.
- Additional V_{SB}-based body-bias tuning suppresses residual curvature, achieving 0.61 ppm /°C TC and 0.3 mV variation from −20°C to 100°C, while AEC-Q100-based validation is planned for future work.

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